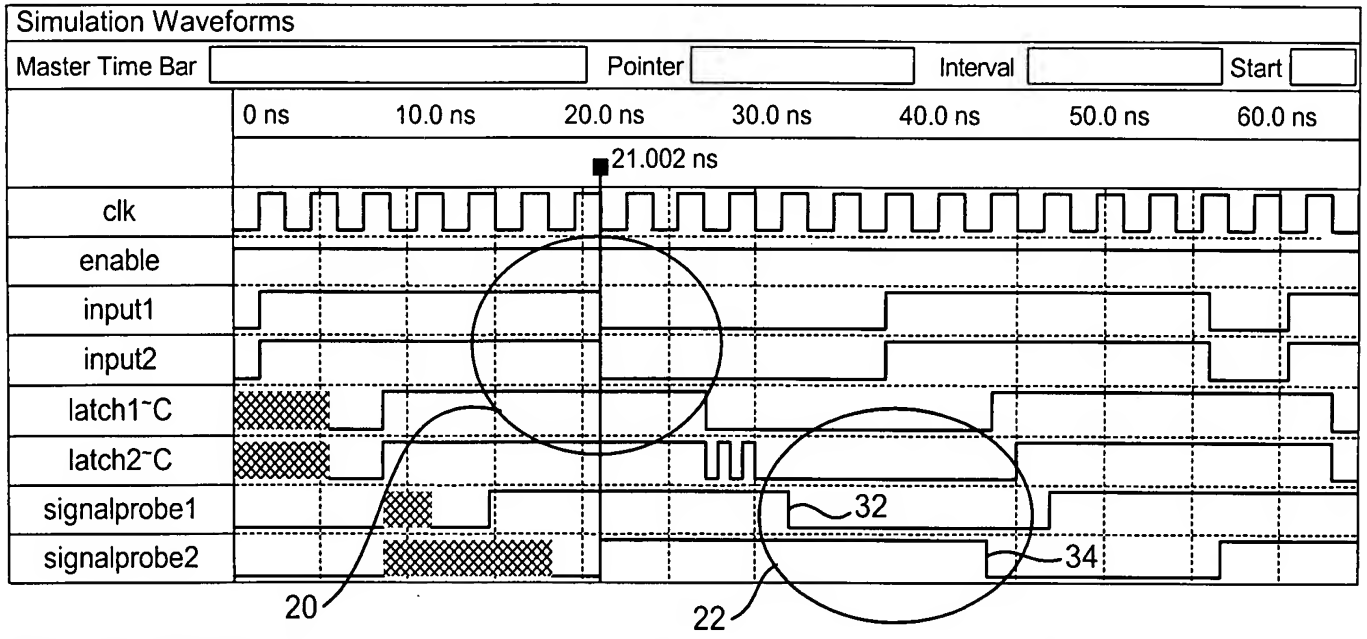


FIG. 1
(PRIOR ART)

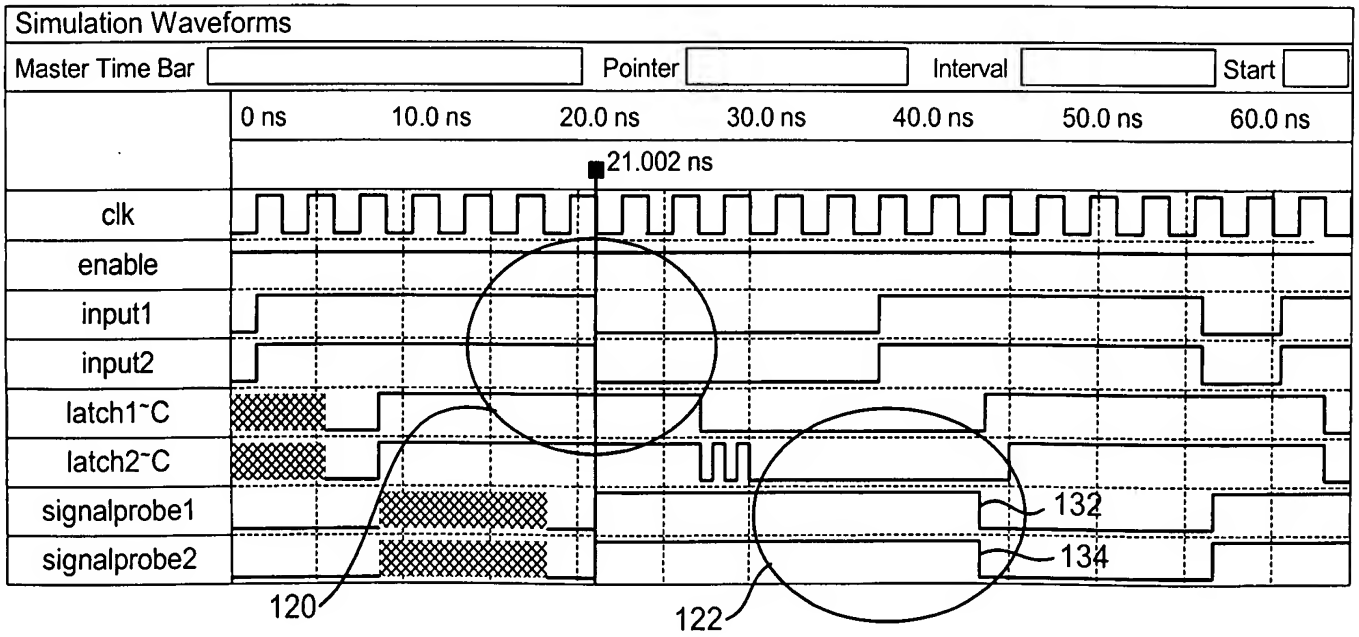


FIG. 2

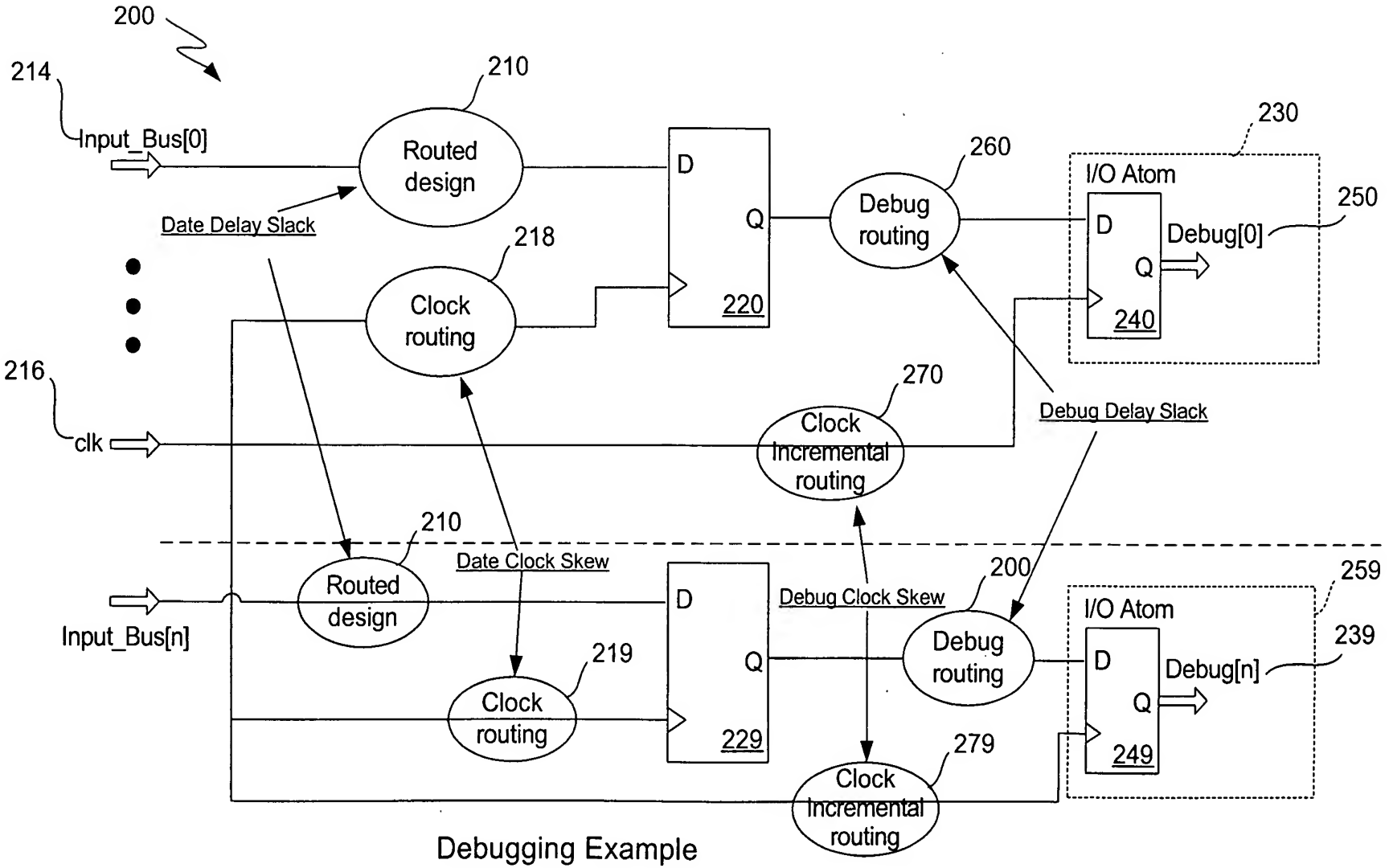

200
214
Input_Bus[0]
210
Routed design
Date Delay Slack
218
Clock routing
D
Q
220
260
Debug routing
230
I/O Atom
D
Q
240
Debug[0]
250
216
clk
270
Clock Incremental routing
Debug Delay Slack
210
Routed design
Input_Bus[n]
Date Clock Skew
219
Clock routing
D
Q
229
Debug Clock Skew
200
Debug routing
259
I/O Atom
D
Q
249
Debug[n]
239
279
Clock Incremental routing
Debugging Example

FIG. 3

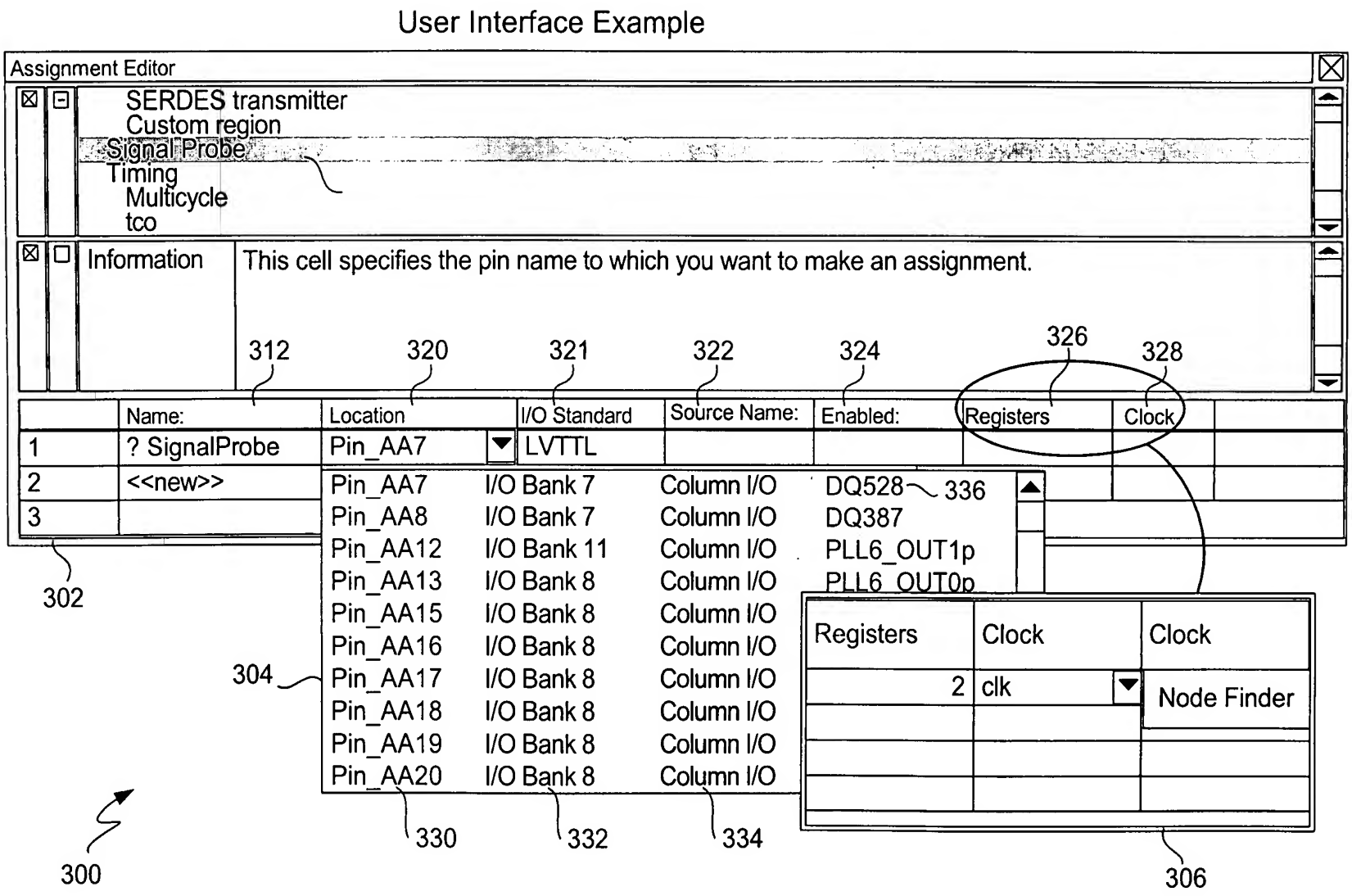

User Interface Example
Assignment Editor
SERDES transmitter
Custom region
Signal Probe
Timing
Multicycle
tco
Information
This cell specifies the pin name to which you want to make an assignment.
312
320
321
322
324
326
328
Name:
Location
I/O Standard
Source Name:
Enabled:
Registers
Clock
1
? SignalProbe
Pin_AA7
LVTTL
2
<<new>>
3
Pin_AA7 I/O Bank 7 Column I/O DQ528
Pin_AA8 I/O Bank 7 Column I/O DQ387
Pin_AA12 I/O Bank 11 Column I/O PLL6_OUT1p
Pin_AA13 I/O Bank 8 Column I/O PLL6_OUT0p
Pin_AA15 I/O Bank 8 Column I/O
Pin_AA16 I/O Bank 8 Column I/O
Pin_AA17 I/O Bank 8 Column I/O
Pin_AA18 I/O Bank 8 Column I/O
Pin_AA19 I/O Bank 8 Column I/O
Pin_AA20 I/O Bank 8 Column I/O
336
302
304
330
332
334
300
Registers
Clock
Clock
2
clk
Node Finder
306

FIG. 4

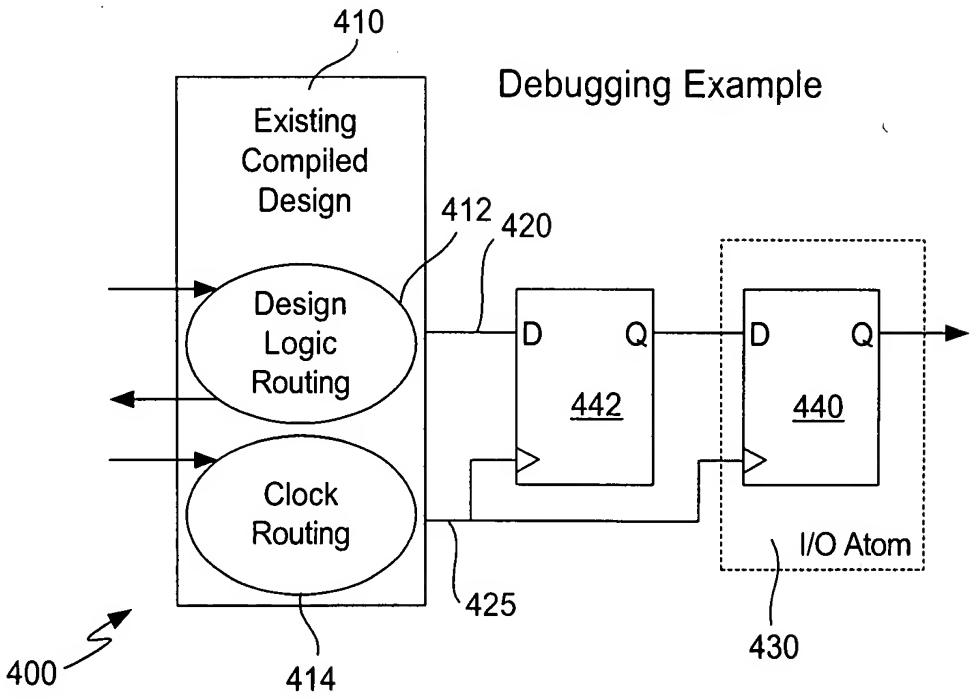

410
Debugging Example
Existing
Compiled
Design
412
420
Design
Logic
Routing
Clock
Routing
D
Q
442
D
Q
440
I/O Atom
425
430
400
414

FIG. 5

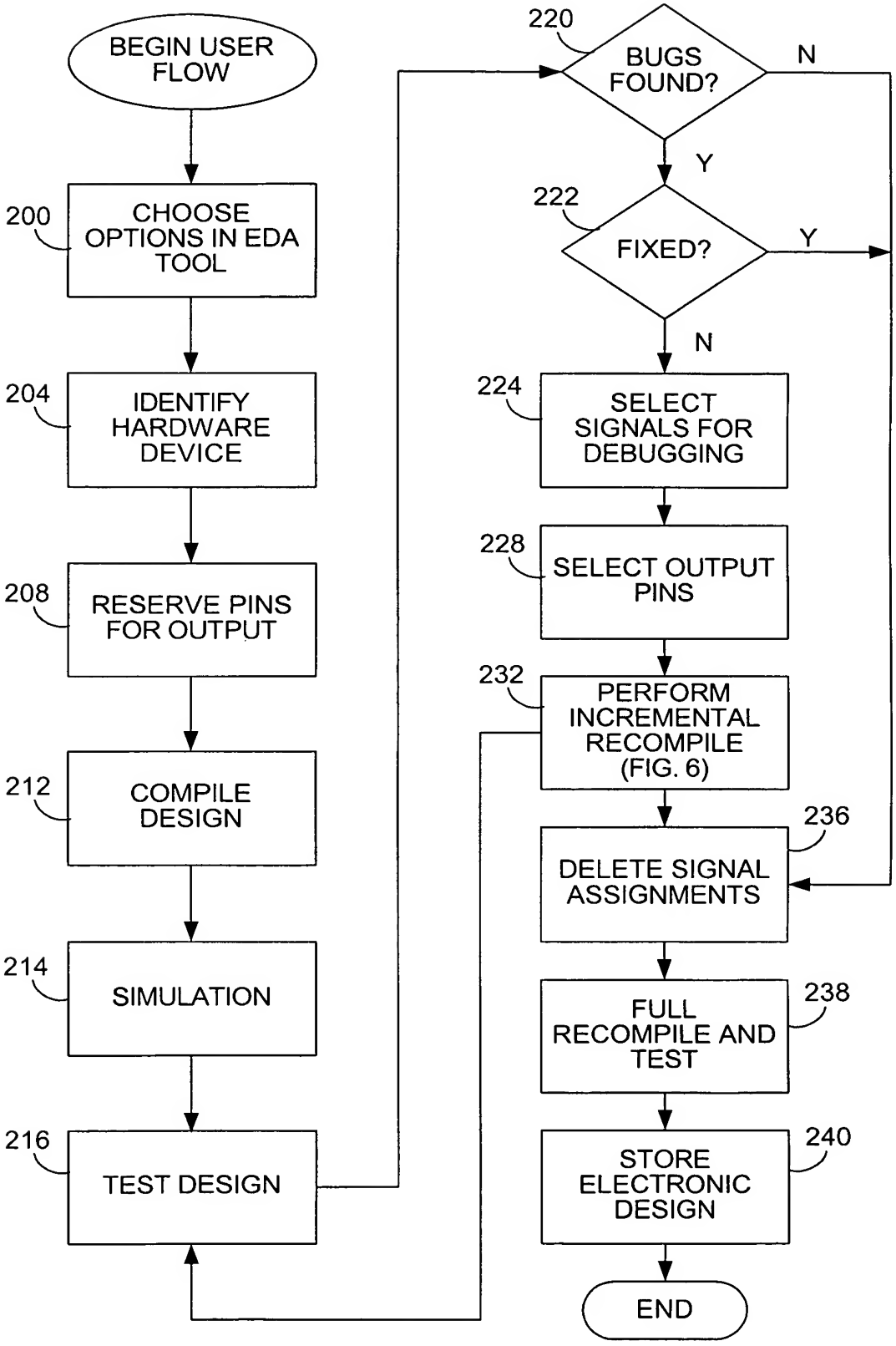

BEGIN USER FLOW
200
CHOOSE OPTIONS IN EDA TOOL
204
IDENTIFY HARDWARE DEVICE
208
RESERVE PINS FOR OUTPUT
212
COMPILE DESIGN
214
SIMULATION
216
TEST DESIGN
220
BUGS FOUND?
N
Y
222
FIXED?
Y
N
224
SELECT SIGNALS FOR DEBUGGING
228
SELECT OUTPUT PINS
232
PERFORM INCREMENTAL RECOMPILE (FIG. 6)
236
DELETE SIGNAL ASSIGNMENTS
238
FULL RECOMPILE AND TEST
240
STORE ELECTRONIC DESIGN
END

FIG. 6

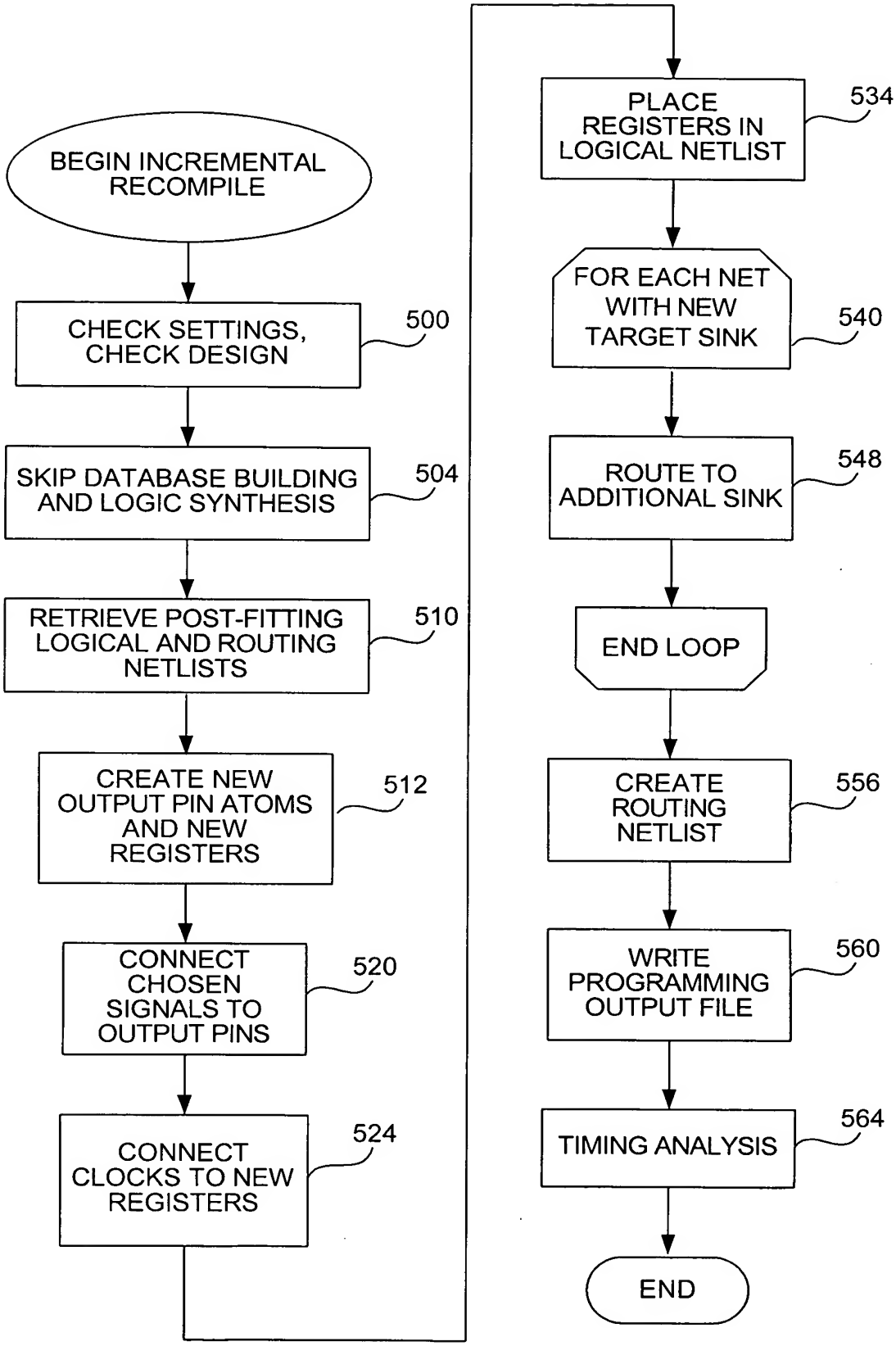

BEGIN INCREMENTAL RECOMPILE
CHECK SETTINGS, CHECK DESIGN
500
SKIP DATABASE BUILDING AND LOGIC SYNTHESIS
504
RETRIEVE POST-FITTING LOGICAL AND ROUTING NETLISTS
510
CREATE NEW OUTPUT PIN ATOMS AND NEW REGISTERS
512
CONNECT CHOSEN SIGNALS TO OUTPUT PINS
520
CONNECT CLOCKS TO NEW REGISTERS
524
PLACE REGISTERS IN LOGICAL NETLIST
534
FOR EACH NET WITH NEW TARGET SINK
540
ROUTE TO ADDITIONAL SINK
548
END LOOP
CREATE ROUTING NETLIST
556
WRITE PROGRAMMING OUTPUT FILE
560
TIMING ANALYSIS
564
END

FIG. 7

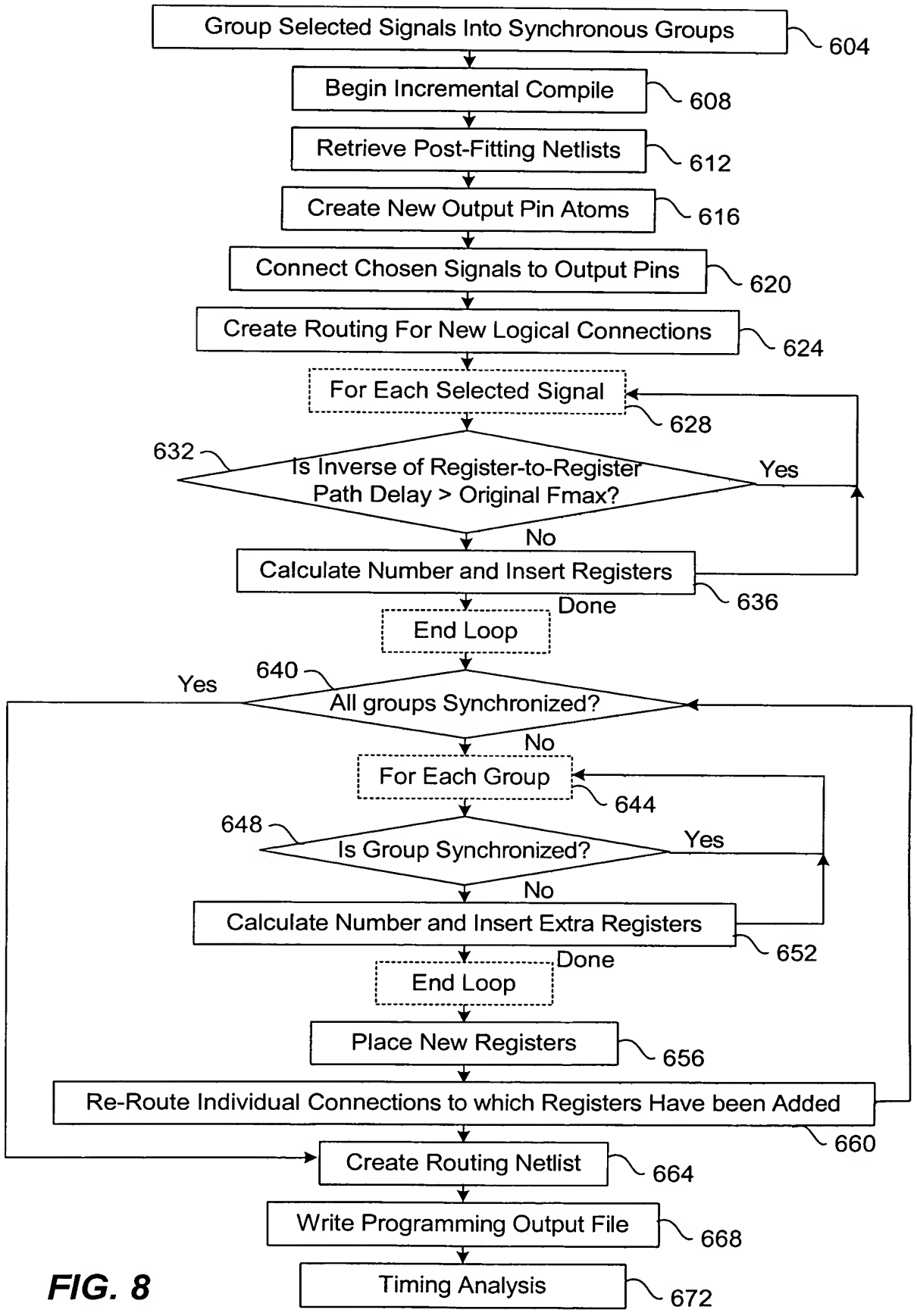
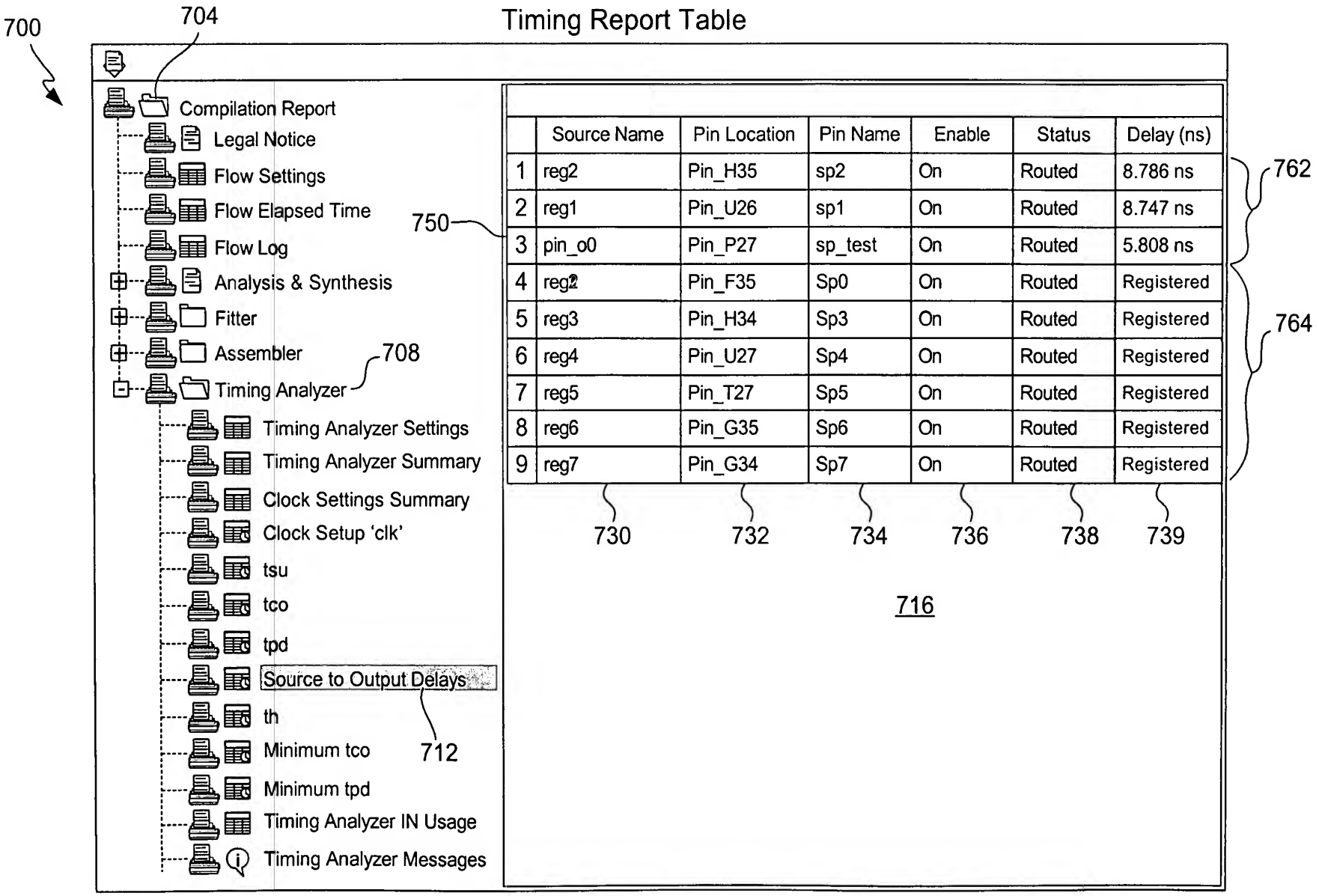

Group Selected Signals Into Synchronous Groups
604
Begin Incremental Compile
608
Retrieve Post-Fitting Netlists
612
Create New Output Pin Atoms
616
Connect Chosen Signals to Output Pins
620
Create Routing For New Logical Connections
624
For Each Selected Signal
628
632
Is Inverse of Register-to-Register Path Delay > Original Fmax?
Yes
No
Calculate Number and Insert Registers
636
Done
End Loop
640
Yes
All groups Synchronized?
No
For Each Group
644
648
Is Group Synchronized?
Yes
No
Calculate Number and Insert Extra Registers
652
Done
End Loop
Place New Registers
656
Re-Route Individual Connections to which Registers Have been Added
660
Create Routing Netlist
664
Write Programming Output File
668
Timing Analysis
672

FIG. 8



	Source Name	Pin Location	Pin Name	Enable	Status	Delay (ns)
1	reg2	Pin_H35	sp2	On	Routed	8.786 ns
2	reg1	Pin_U26	sp1	On	Routed	8.747 ns
3	pin_o0	Pin_P27	sp_test	On	Routed	5.808 ns
4	reg2	Pin_F35	Sp0	On	Routed	Registered
5	reg3	Pin_H34	Sp3	On	Routed	Registered
6	reg4	Pin_U27	Sp4	On	Routed	Registered
7	reg5	Pin_T27	Sp5	On	Routed	Registered
8	reg6	Pin_G35	Sp6	On	Routed	Registered
9	reg7	Pin_G34	Sp7	On	Routed	Registered

FIG. 9

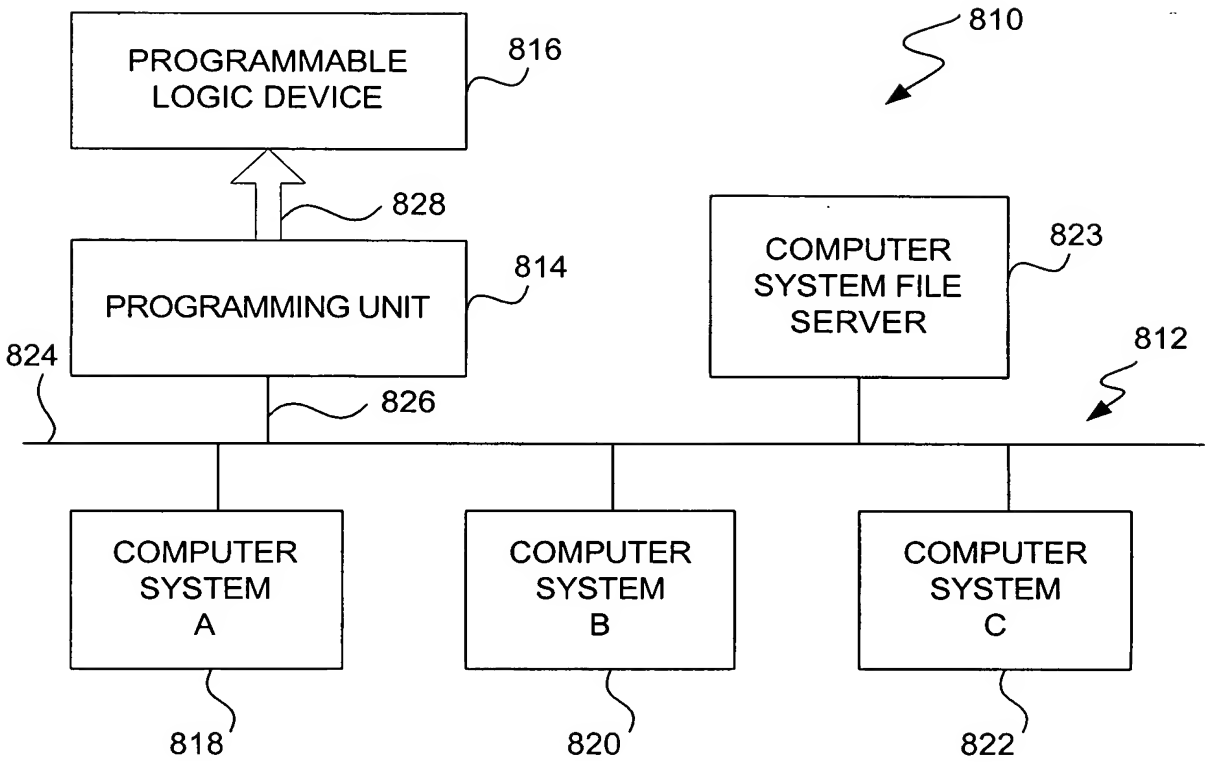

PROGRAMMABLE LOGIC DEVICE
816
810
828
COMPUTER SYSTEM FILE SERVER
823
PROGRAMMING UNIT
814
812
824
826
COMPUTER SYSTEM A
COMPUTER SYSTEM B
COMPUTER SYSTEM C
818
820
822

FIG. 10

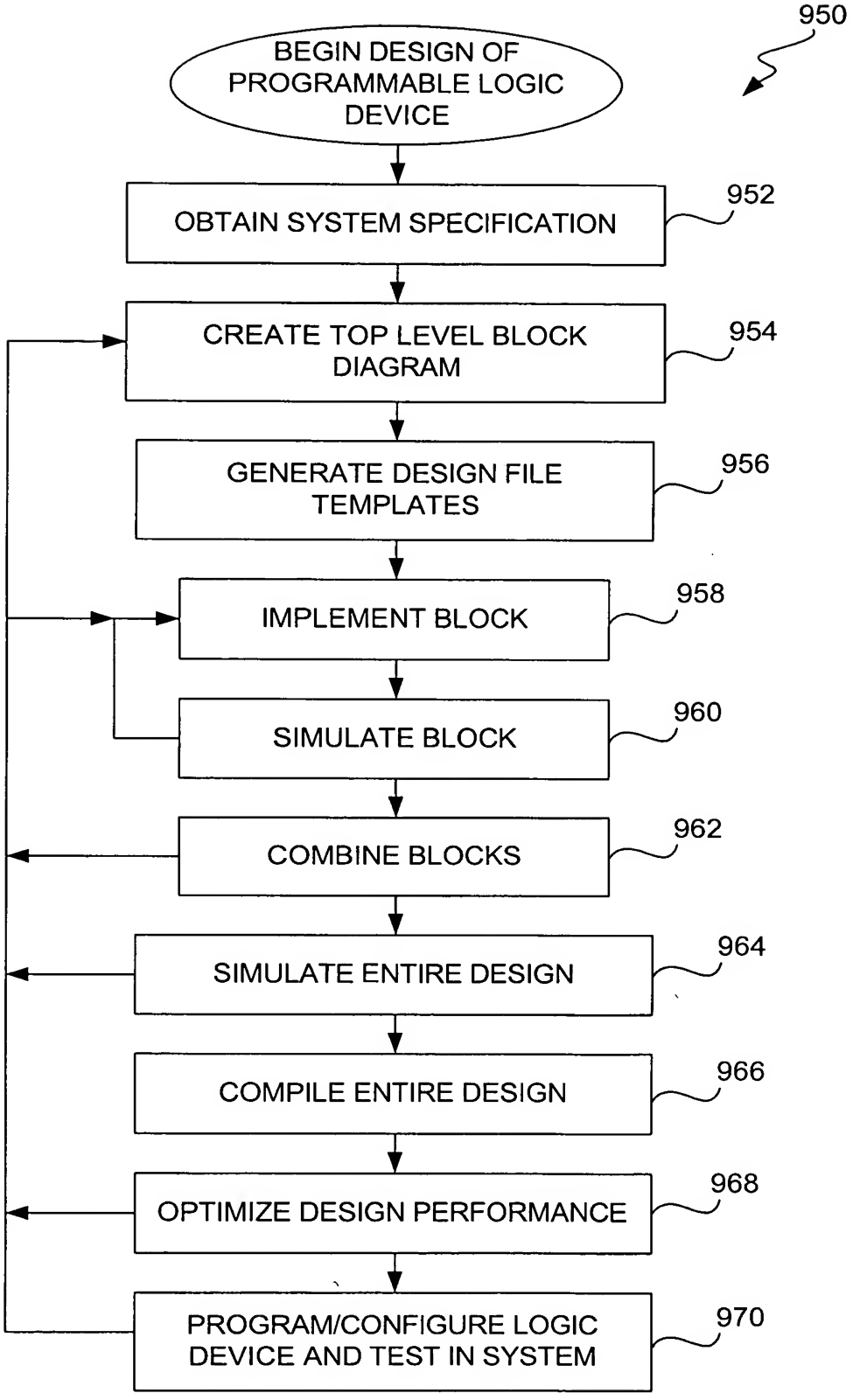

950
BEGIN DESIGN OF PROGRAMMABLE LOGIC DEVICE
OBTAIN SYSTEM SPECIFICATION
952
CREATE TOP LEVEL BLOCK DIAGRAM
954
GENERATE DESIGN FILE TEMPLATES
956
IMPLEMENT BLOCK
958
SIMULATE BLOCK
960
COMBINE BLOCKS
962
SIMULATE ENTIRE DESIGN
964
COMPILE ENTIRE DESIGN
966
OPTIMIZE DESIGN PERFORMANCE
968
PROGRAM/CONFIGURE LOGIC DEVICE AND TEST IN SYSTEM
970

FIG. 11

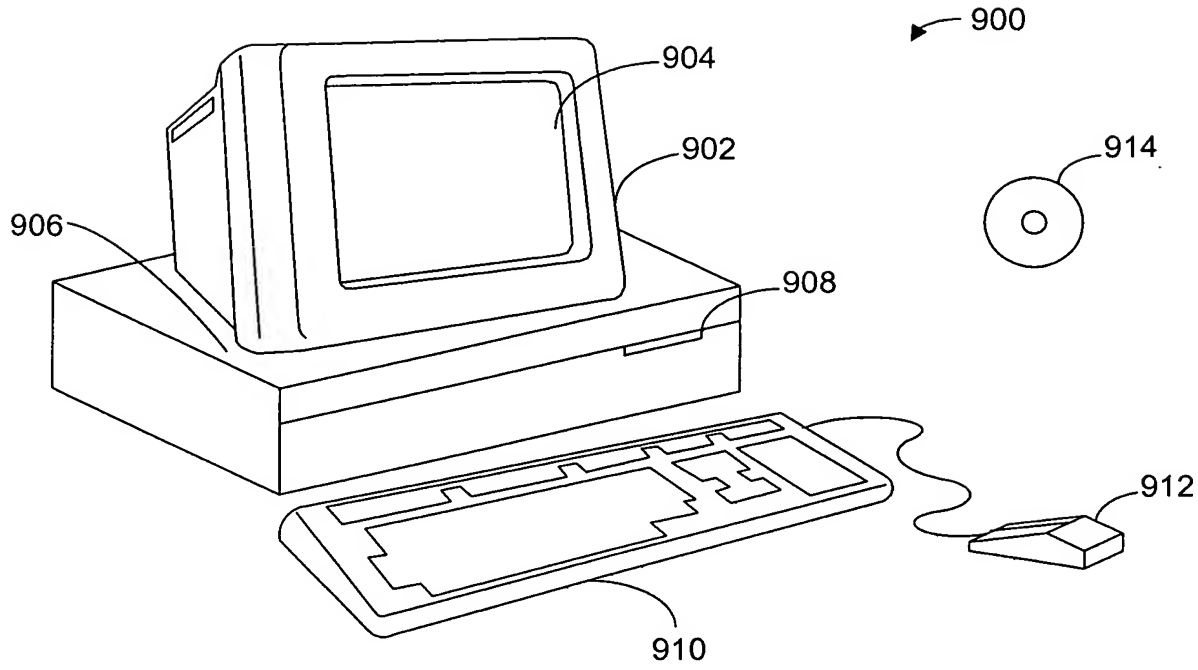


FIG. 12A

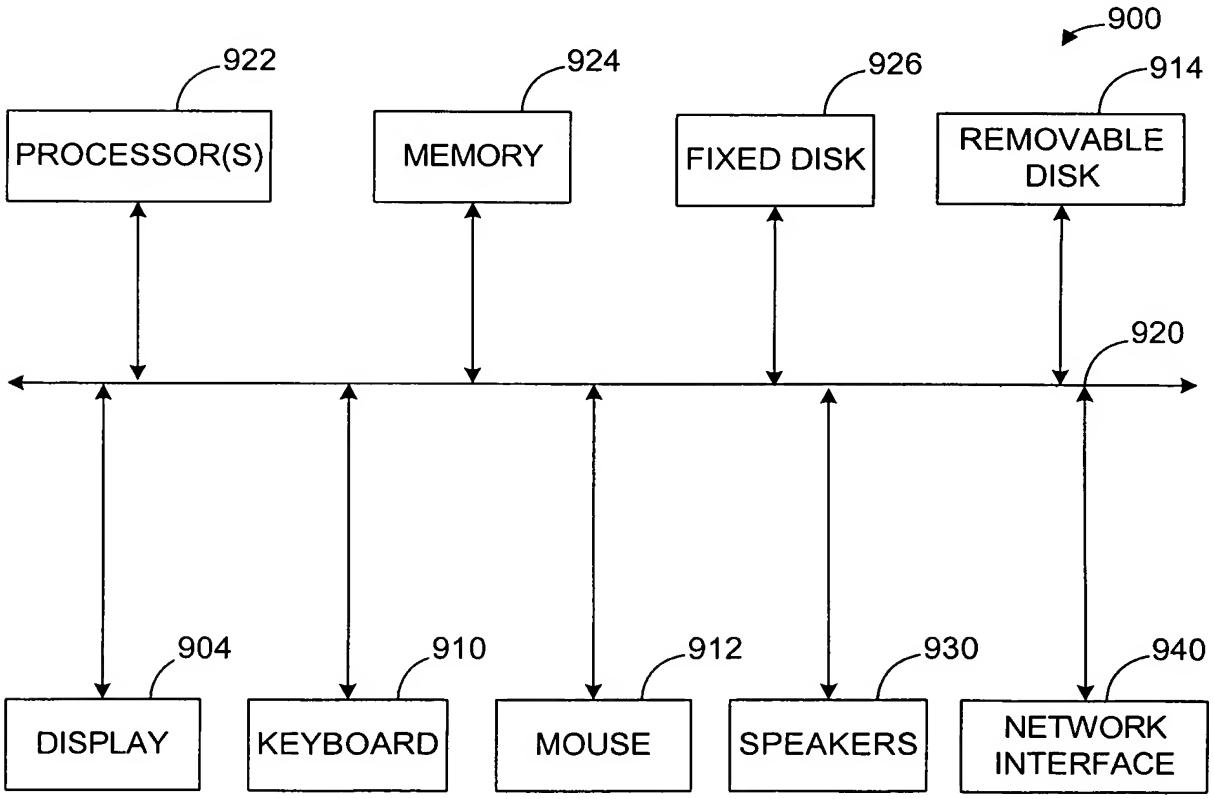


FIG. 12B